FIN CAPACITOR

DESCRIPTION

[Para 1] BACKGROUND OF THE INVENTION

[Para 2] Field of the Invention

[Para 3] The invention generally relates to a capacitor structure and method for forming the same and more particularly to a capacitor structure that has a conductive substrate, conductive fins extending above the substrate, and trenches extending into the substrate.

[Para 4] Description of the Related Art

[Para 5] Capacitors are one of the fundamental components in today's electronic devices and operate by storing a charge. For example, capacitors are often used in dynamic random access memory (DRAM) and other similar devices. One type of common capacitor uses an upper plate and a lower plate that are separated by an insulator. The invention described below provides a new type of capacitor that is substantially smaller, faster, and less-expensive to manufacture than conventional capacitors.

[Para 6] SUMMARY OF THE INVENTION

[Para 7] Disclosed is a capacitor structure and method for forming the same. This structure has a conductive substrate, conductive fins extending above the substrate, and trenches extending into the substrate. These

trenches are positioned between locations where the fins extend above the substrate. The invention includes an insulator in the trenches and covering the fins. This insulator separates the substrate and fins from a conductive top plate that covers the fins and fills the trenches. A bottom plate contact electrically connects the fins and the substrate such that the fins and the substrate comprise a bottom plate of the capacitor structure.

[Para 8] In one embodiment, the fins and the substrate act as the bottom plate of the capacitor. In a second embodiment, only the substrate acts as the bottom plate of the capacitor and the fins are electrically isolated from the substrate and from the top plate of the capacitor. In another embodiment, the fins are used to pattern the trenches in the substrate.

[Para 9] The invention can be formed in any type of common integrated structure, such as in the bulk portion of the integrated chip substrate or in a silicon-on-insulator (SOI) type structure. In the SOI structure, the fins extend from the insulator layer that covers the substrate and can include conductive spacers on the fins that electrically connect the fins to the substrate. The insulator that covers the fins and lines the trenches can be separated by the SOI insulator layer and therefore this insulator comprises a first insulator portion lining the trenches and a second insulator portion covering the fins. Also, the bottom plate contact is insulated from the top plate.

[Para 10] This structure is formed using one or more methods that pattern the conductive fins above the conductive substrate (e.g., on the doped bulk substrate or on the insulator layer of an SOI structure). The invention then forms trenches to extend into the substrate between locations where the fins extend above the substrate. One or more insulators are then formed in the trenches and on the fins. The conductive top plate is then formed on the fins and to fill the trenches. The bottom plate can be formed at the same time (or later) and the bottom plate contact electrically connects the fins and the substrate to form a bottom plate of the capacitor structure. In SOI structures, the invention can also form conductive spacers on the fins to electrically connect the fins to the substrate. When forming the fins, the invention

patterns an insulating mask on a conductive layer and then patterns the conductive fins through the insulating mask. The mask remains as a permanent part of the structure and helps to insulate the fins from the overlying top plate.

[Para 11] These, and other, aspects and objects of the present invention will be better appreciated and understood when considered in conjunction with the following description and the accompanying drawings. It should be understood, however, that the following description, while indicating preferred embodiments of the present invention and numerous specific details thereof, is given by way of illustration and not of limitation. Many changes and modifications may be made within the scope of the present invention without departing from the spirit thereof, and the invention includes all such modifications.

[Para 12] BRIEF DESCRIPTION OF THE DRAWINGS

[Para 13] The invention will be better understood from the following detailed description with reference to the drawings, in which:

[Para 14] Figure 1 is a schematic cross-sectional diagram of a partially completed capacitor according to the invention;

[Para 15] Figure 2 is a schematic cross-sectional diagram of a partially completed capacitor according to the invention;

[Para 16] Figure 3 is a schematic cross-sectional diagram of a partially completed capacitor according to the invention;

[Para 17] Figure 4 is a schematic cross-sectional diagram of a partially completed capacitor according to the invention;

[Para 18] Figure 5 is a schematic cross-sectional diagram of a partially completed capacitor according to the invention;

[Para 19] Figure 6 is a schematic top-view diagram of a partially completed capacitor according to the invention;

[Para 20] Figure 7 is a schematic cross-sectional diagram of a partially completed capacitor according to the invention;

[Para 21] Figure 8 is a schematic top-view diagram of a partially completed capacitor according to the invention;

[Para 22] Figure 9 is a schematic cross-sectional diagram of a partially completed capacitor according to the invention;

[Para 23] Figure 10 is a schematic cross-sectional diagram of a partially completed capacitor according to the invention;

[Para 24] Figure 11 is a schematic top-view diagram of a partially completed capacitor according to the invention;

[Para 25] Figure 12 is a schematic cross-sectional diagram of a partially completed capacitor according to the invention;

[Para 26] Figure 13 is a schematic cross-sectional diagram of a partially completed capacitor according to the invention;

[Para 27] Figure 14 is a schematic top-view diagram of a partially completed capacitor according to the invention;

[Para 28] Figure 15 is a schematic cross-sectional diagram of a partially completed capacitor according to the invention;

[Para 29] Figure 16 is a schematic cross-sectional diagram of a partially completed capacitor according to the invention;

[Para 30] Figure 17 is a schematic top-view diagram of a partially completed capacitor according to the invention;

[Para 31] Figure 18 is a schematic cross-sectional diagram of a partially completed capacitor according to the invention;

[Para 32] Figure 19 is a schematic cross-sectional diagram of a partially completed capacitor according to the invention;

[Para 33] Figure 20 is a schematic cross-sectional diagram of a partially completed capacitor according to the invention;

[Para 34] Figure 21 is a schematic cross-sectional diagram of a partially completed capacitor according to the invention;

[Para 35] Figure 22 is a schematic cross-sectional diagram of a partially completed capacitor according to the invention;

[Para 36] Figure 23 is a schematic top-view diagram of a partially completed capacitor according to the invention;

[Para 37] Figure 24 is a schematic cross-sectional diagram of a partially completed capacitor according to the invention;

[Para 38] Figure 25 is a schematic cross-sectional diagram of a partially completed capacitor according to the invention;

[Para 39] Figure 26 is a schematic cross-sectional diagram of a partially completed capacitor according to the invention;

[Para 40] Figure 27 is a schematic cross-sectional diagram of a partially completed capacitor according to the invention;

[Para 41] Figure 28 is a schematic top-view diagram of a partially completed capacitor according to the invention;

[Para 42] Figure 29 is a schematic cross-sectional diagram of a partially completed capacitor according to the invention;

[Para 43] Figure 30 is a schematic cross-sectional diagram of a partially completed capacitor according to the invention;

[Para 44] Figure 31 is a schematic top-view diagram of a partially completed capacitor according to the invention;

[Para 45] Figure 32 is a schematic cross-sectional diagram of a partially completed capacitor according to the invention;

[Para 46] Figure 33 is a schematic cross-sectional diagram of a partially completed capacitor according to the invention;

[Para 47] Figure 34 is a schematic top-view diagram of a partially completed capacitor according to the invention;

[Para 48] Figure 35 is a schematic top-view diagram of a partially completed capacitor according to the invention; and

[Para 49] Figure 36 is a flow diagram illustrating a preferred method of the invention.

[Para 50] DETAILED DESCRIPTION OF PREFERRED EMBODIMENTS OF THE INVENTION

[Para 51] The present invention and the various features and advantageous details thereof are explained more fully with reference to the nonlimiting embodiments that are illustrated in the accompanying drawings and detailed in the following description. It should be noted that the features illustrated in the drawings are not necessarily drawn to scale. Descriptions of well-known components and processing techniques are omitted so as to not unnecessarily obscure the present invention. The examples used herein are intended merely to facilitate an understanding of ways in which the invention may be practiced and to further enable those of skill in the art to practice the invention. Accordingly, the examples should not be construed as limiting the scope of the invention.

[Para 52] As mentioned above, the invention provides a new type of capacitor (e.g., memory capacitor such as a DRAM capacitor) that is substantially smaller, faster, and less-expensive to manufacture than conventional capacitors. In addition, the invention offers a substantial

increase in capacitor surface area, which dramatically increases the capacitance of the capacitor. One example of the inventive structure is shown in Figures 15-17. Figures 1-17 (discussed in greater detail below) illustrate one methodology for forming this inventive structure. Figures 15 and 16 are cross-sectional views and Figure 17 is a top-view. Figure 15 is a cross-sectional view drawn along line I-I' in Figure 17, while Figure 16 is a cross-sectional view drawn along line II-II' in Figure 17.

[Para 53] The structure shown in Figures 15-17 has a conductive substrate 10, conductive fins 30 extending above the substrate 10, and trenches 42 extending into the substrate 10. These trenches 42 are positioned between locations where the fins 30 extend above the substrate 10. The invention includes an insulators 70, 72 in the trenches 42 and covering the fins 30. This insulators 70, 72 separates the substrate 10 and fins 30 from a conductive top plate 160 that covers the fins 30 and fills the trenches 42. A bottom plate contact 170 electrically connects the fins 30 and the substrate 10 such that the fins 30 and the substrate 10 comprise a bottom plate of the capacitor structure.

[Para 54] More specifically, this process begins in Figure 1 where a substrate 10 is implanted with an impurity 12. This impurity 12 can be any type of well-known impurity that changes the substrate 10 into a conductor. For example, the impurity 12 can comprise boron, phosphorus, arsenic, or other similar impurities. As would be understood by one ordinarily skilled in the art, the actual impurity and impurity concentrations used will vary depending upon the material makeup of the substrate. Alternatively, rather than implanting an impurity into a substrate, a conductive substrate can be formed, thereby eliminating the need to implant an impurity. However, by implanting an impurity, the invention can be used with a broader variety of devices, especially if only a portion of the substrate 10 is transformed into a conductor. By masking the substrate so that only portions of the substrate where the inventive capacitors will be formed are made conductive, other portions of the substrate can remain as insulators to be used with other types of devices. Well-known masking techniques can be used to distinguish which

regions of the substrate 10 will become conductive and will be used for the inventive capacitor structure.

[Para 55] In Figure 2, an insulator 20 such as an oxide, nitride, etc. is deposited over the substrate 10 and a conductive layer 22 is formed over the insulator 20. In one embodiment, the conductive layer 22 comprises polysilicon (or doped silicon). To the contrary, the conductor 22 can comprise any well-known conductor, including metals, alloys, conductively doped material, etc. An insulating mask 24 is patterned over the conductive layer 22 using any well-known patterning techniques such as photolithographic techniques. In the preferred embodiment the conductive layer 22 comprises doped silicon, formed over the insulator 20 by one of the well-known Silicon-On-Insulator techniques, such as Bond-and-Etch-Back, or SIMOX.

[Para 56] In Figure 3, the mask 24 is used to pattern the conductor 22 into conductive fins 30. For example, a directional etching process (or any well-known material removal process) can be utilized to pattern the conductor layer 22 into the fins 30. Next, as shown in Figure 4, the same material removal process can be continued, or an additional material removal processes can be utilized to pattern the insulator 20 and substrate 10 to form the trenches 42 shown in Figure 4.

[Para 57] Note that in Figure 4 an additional mask 40 is utilized to protect the areas of the insulator layer 20 that are not to be patterned. In Figure 5, the additional mask 40 is removed; however, the insulating mask 24 remains above the fins 30 and will remain in the final structure to insulate the fins 30 from the overlying top plate 160. Figure 6 illustrates a top-view of the structure shown in Figure 5, where the structure in Figure 5 is a cross-sectional view along line I-I'.

[Para 58] In Figure 7, insulators 70, 72 are formed along the sidewalls of the fins 30 and along the trenches 42. These insulators 70, 72 can be the same insulator or different insulators, depending upon the specific design and materials being utilized. The insulators 70, 72 can be formed in a single step or multiple steps, again depending upon the specifics of the design in

question. For example, the insulators 70, 72 can be an oxide that is grown upon the fins 30 and in the trenches 42, or the insulators 70, 72 can be deposited conformally over the structure. Again, Figure 8 is a top-view of Figure 7, with Figure 7 being the cross-section shown along line I-I'.

[Para 59] In Figures 9-11, the invention utilizes a mask 90 to selectively remove portions of the insulators 70, 72. More specifically, Figure 11 is a top-view, Figure 9 is a cross-sectional view drawn along line I-I', while Figure 10 is a cross-sectional view drawn along line II-II'. The mask 90 allows the portion of the structure shown in Figure 10 to be exposed while the remaining portion shown in Figure 9 is protected. Then, a material removal processes such as chemical etching, reactive-ion etching, heating, etc. is utilized to remove the exposed portions of the insulators 70, 72. The actual material removal process that will be used depends upon the specific type of material that was used for the insulators 70, 72. This results in the structures shown in Figures 12-14, where the insulators 70, 72 is no longer present in the cross-section II-II' of Figure 14 (shown in Figure 13) while the insulators 70, 72 is still present in the cross section I-I' of Figure 14 (shown in Figure 12).

[Para 60] The mask 90 is then removed and a conductor is patterned over the structure to form the top plate 160 and the bottom plate contact 170. Once again, Figure 15 is a cross-sectional view alone line I-I' of Figure 17, and Figure 16 is a cross-sectional view along line II-II' of Figure 17. As can be seen in the drawings, the bottom plate contact 170 electrically connects the fins 30 and the conductive substrate 10 because there is no insulator surrounding the fins 30 or the trenches 42 in the region where the bottom plate contact 170 is formed. To the contrary, the fins 30 and conductive substrate 10 are insulated from the top plate contact 160 by the insulators 70, 72 and the insulating layer 20. This capacitor structure will eventually be completed by depositing an insulator between the upper plate 160 and the bottom plate contact 170. For example, Figure 35 illustrates an insulator 360 between the top plate 160 and the bottom plate contact 170. Figure 17 also illustrates the control device 180 (such as a transistor, etc.) that allows

selective access to the bottom line contact 170, for example, to store charge or read the charge within the memory capacitor.

[Para 61] Figures 18-23 illustrate another embodiment of the invention that is formed in the bulk area of the substrate, as opposed to the SOI structure shown in Figures 1-17. The processing shown in Figures 18-23 is somewhat similar to that shown in Figures 1-17 except that the insulator layer 20 is not utilized in the processing steps or structure shown in Figures 18-23. Instead, the invention begins by implanting the impurity 12 into a bulk substrate 190 (as opposed to the SOI substrate 10 that is discussed above). Then, the same conductor 22 and mask 24 described above in Figure 23 are utilized to form the fins 30 in Figure 20 as was done in Figure 3, above. The same processing steps shown in Figures 4-17 are then used to complete the structure which results in the structure shown in Figures 21-23. More specifically, Figures 21-23 are substantially similar to Figures 15-17, except that in Figures 21-23 no insulator layer 20 is present. Further, in Figures 21-23 the substrate 190 is a bulk substrate. Otherwise, structure and processing shown are similar to those discussed above and a redundant discussion of the same as avoided.

[Para 62] Thus, as shown above, the invention can be formed in any type of common integrated structure, such as in the bulk portion of the integrated chip substrate (Figures 21-23) or in a silicon-on-insulator (SOI) type structure (Figures 15-17). In the SOI structure, the fins 30 extend from the insulator layer that covers the substrate 10 and can include conductive spacers on the fins 30 that electrically connect the fins 30 to the substrate 10. The insulator that covers the fins 30 and lines the trenches 42 can be separated by the SOI insulator layer and therefore this insulator comprises a first insulator portion lining the trenches 42 and a second insulator portion covering the fins 30. Also, the bottom plate contact is insulated from the top plate.

[Para 63] Figures 24-31 illustrate another embodiment of the invention. In the embodiment shown in Figures 24-31, a portion of the insulator 70 along sides of the fins 30 is intentionally removed to place the fins 30 in

contact with the top plate 160. Therefore, in this embodiment, the lower plate comprises only the substrate 10 and does not utilize any part of the fins 30 as the lower plate. Instead, the fins 30 are used to pattern the trenches 42. As shown in Figure 24, after the processing shown in Figures 7 and 8 are completed, a protective layer 250 is formed to protect the insulator 72 and potentially a portion of the insulator 70. Whether the entire insulator 70 is removed depends upon the specific implementation of the invention and whether the insulator layer 20 supplies a sufficient amount of insulation on its own. If it does not, some of the insulator 70 is left to remain on the lower portion of the fins 30. Then, with the protective layer 250 in place, the exposed portions of the insulator 70 are removed. Next, the protective material is removed resulting in the structure shown in Figure 25.

[Para 64] Then, as shown in Figures 26-28, a mask 290 is formed which protects the region shown in Figure 26 and allows the region shown in Figure 27 to be exposed. Once again, as with the previous drawings, Figure 26 is a cross-sectional view along line I-I' in Figure 28, and Figure 27 is a cross-sectional view along line II-II' in Figure 28. With the mask 290 in place, the fins 30 are removed from the area not protected by the mask, as shown in Figure 27. Once again, the specific material removal process will depend upon the material makeup of the fins 30 and can include etching, chemical processing, etc.

[Para 65] The structure then undergoes the processing discussed above in Figures 15-17 to form the structure shown in Figures 29-31. Again, Figure 29 is a cross-sectional view along line I-I' and Figure 30 is a cross-sectional view along line II-II' of Figure 31. Note that the bottom plate contact 170 is only in electrical contact with the substrate 10 because the fins have been removed in the processing shown in Figure 27 from the area where the bottom plate contact 170 will be formed. Therefore, as discussed above, in this embodiment, only the substrate 10 is used for the bottom plate and the fins 30 are used to pattern the trenches 42.

[Para 66] Figures 32-34 illustrates another embodiment that avoids the need for a bottom plate contact. Figures 32 and 33 are cross-sectional views along line I-I' in Figure 34. In this embodiment, conductive sidewall spacers 330 are formed as shown in Figure 32 electrically connecting the substrate 10 and the fins 30. This processing is performed after the processing shown in Figure 3. Many different processes can be used to form the sidewall spacers 330. For example, a conductive material can be deposited and then etched in a direction etch that removes material from horizontal surfaces faster than it removes material from vertical surfaces, which leaves the sidewall spacers 330 remaining on the lower portion of the fins. Then, the processing shown in Figures 4-17 would be performed, as discussed above, resulting in the structure shown in Figures 33 and 34. The processing is substantially similar to that discussed above, except that the bottom plate contact 170 does not need to be formed because the fins 30 and substrate 10 are electrically connected by the sidewall spacers 330. Therefore, in Figure 34, only a contact to the substrate 350 is needed to make contact with the lower plate and only the upper plate 160 conductor is illustrated.

[Para 67] Figure 35 can be used with any of the previous embodiments and illustrates the insulator 360 that will eventually cover the bottom plate contact, upper plate, as well as any of the other contacts formed with the invention.

[Para 68] As shown in flowchart form in Figure 36, this structure is formed using one or more methods that pattern the conductive fins above the conductive substrate 370 (e.g., on the doped bulk substrate or on the insulator layer of an SOI structure). The invention then forms trenches 372 that extend into the substrate between locations where the fins extend above the substrate. One or more insulators are then formed in the trenches and on the fins in item 374. The conductive top plate is then formed on the fins and to fill the trenches in item 376. The bottom plate contact can be formed (378) at the same time (or later) and the bottom plate contact electrically connects the fins and the substrate to form a bottom plate of the capacitor structure. In SOI structures, the invention can also form conductive spacers on the fins to

electrically connect the fins to the substrate. When forming the fins, the invention patterns an insulating mask on a conductive layer and then patterns the conductive fins through the insulating mask. The mask remains as a permanent part of the structure and helps to insulate the fins from the overlying top plate.

[Para 69] The invention provides a new type of capacitor (e.g., memory capacitor such as a DRAM capacitor) that is substantially smaller, faster, and less-expensive to manufacture than conventional capacitors. In addition, the invention offers a substantial increase in capacitor surface area, which dramatically increases the capacitance of the capacitor. The invention can thus be produced at a lower cost, and can provide a higher density of memory capacitors. The invention can also use a lower the power consumption of the memory array. Further, this improved structure performs at a higher speed, and can produce a soft error rate improvement.

[Para 70] While the invention has been described in terms of preferred embodiments, those skilled in the art will recognize that the invention can be practiced with modification within the spirit and scope of the appended claims.